MULTIPLICATION REMAINDER ARITHMETIC CIRCUIT

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Abstract of **JP11212951**

PROBLEM TO BE SOLVED: To construct in a practical circuit scale even in the case of handling data that have the large number of digits by using an operation method which repeatedly performs 1-bit partial operation and remainder operation.

SOLUTION: After data A, B and P are set in registers 11, 12 and 17 respectively, if the most significant bit of the B is one in an EOR gate 14 in an initial state, the EOR between the storage data W in an register 15 and the A is calculated. The EOR between output zero of an FF 19 and an output of the gate 14 is calculated in an EOR gate 16. In the next clock cycle, value W obtd. by shifting an output of the gate 16 by one bit to the left is set in the register 15 and also, the most significant bit of an output D of the gate 16 is set in the FF 19. Also, a selector 18 is controlled by an output of the FF 19 in the gate 16, and if an output of the FF 19 is one, the EOR between outputs C and P is calculated. Subsequently, the same operation is repeated and a multiplication remainder is calculated.